Status of the Front End Electronics for the ATLAS Cathode Strip Chambers

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Outline

- On-detector boards
- Off-detector boards
- ASICs needed for on-detector boards
- Low voltage power, cabling
- Faraday cage
- Summary

Board Design for the CSC Electronics

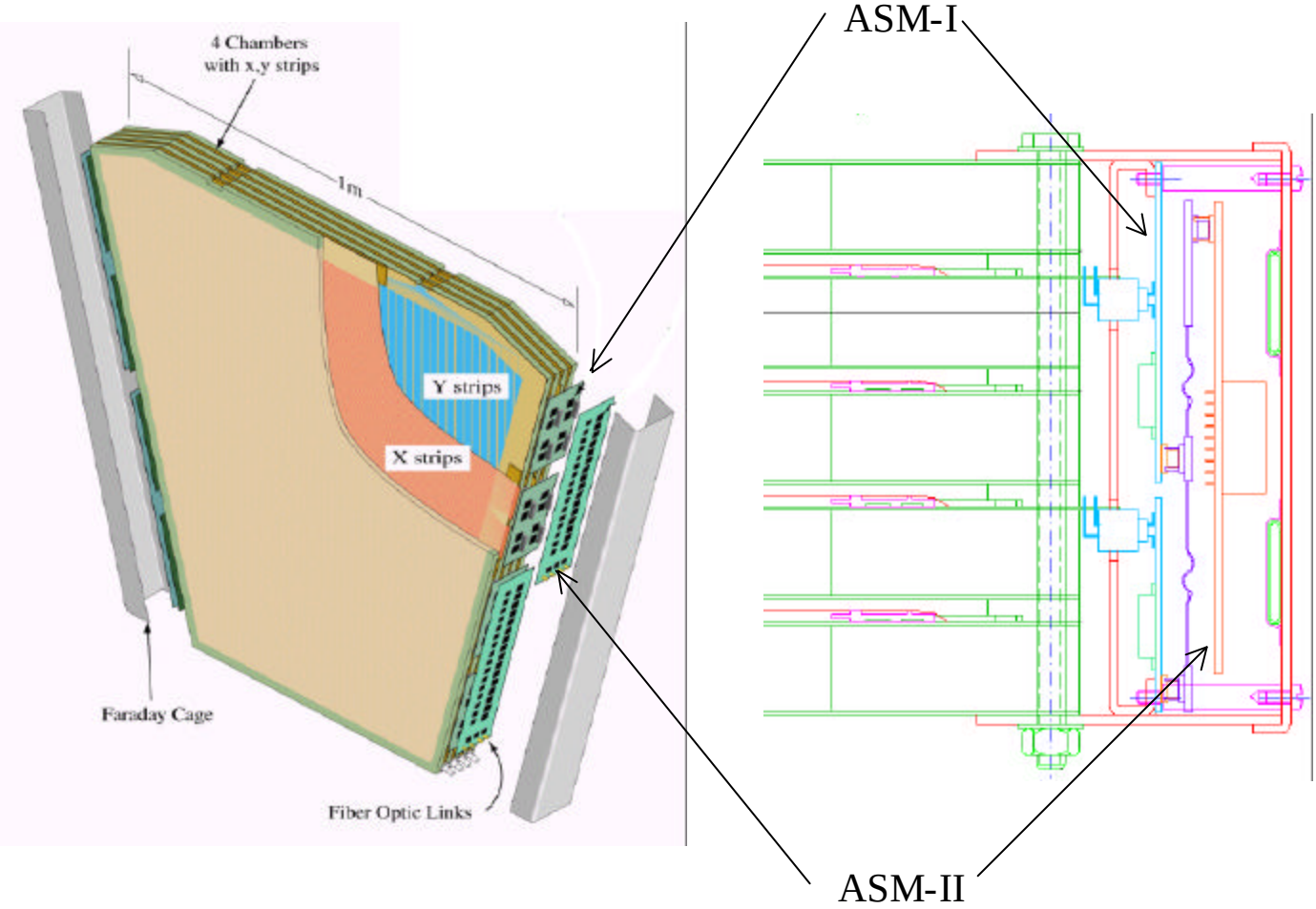
On-detector

- ASM-1
- ASM-2

Off-detector

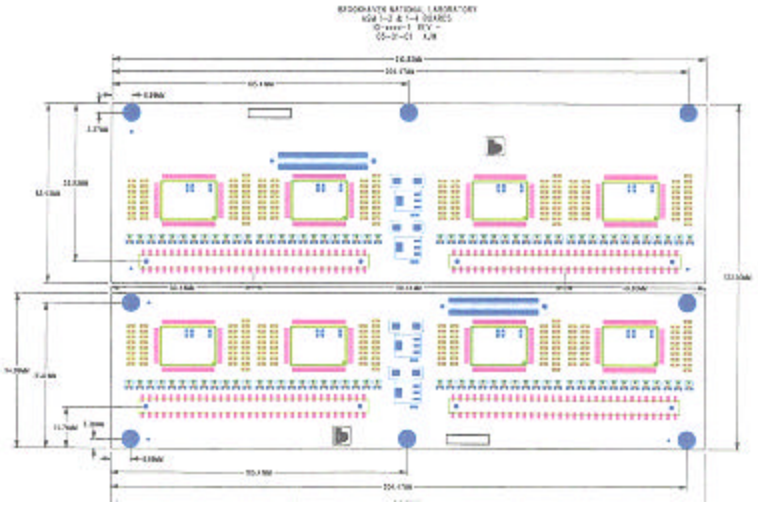
- Sparsifier/ROD
- Concentrator
- Support electronics boards

On-chamber electronics location



ASM-1 board

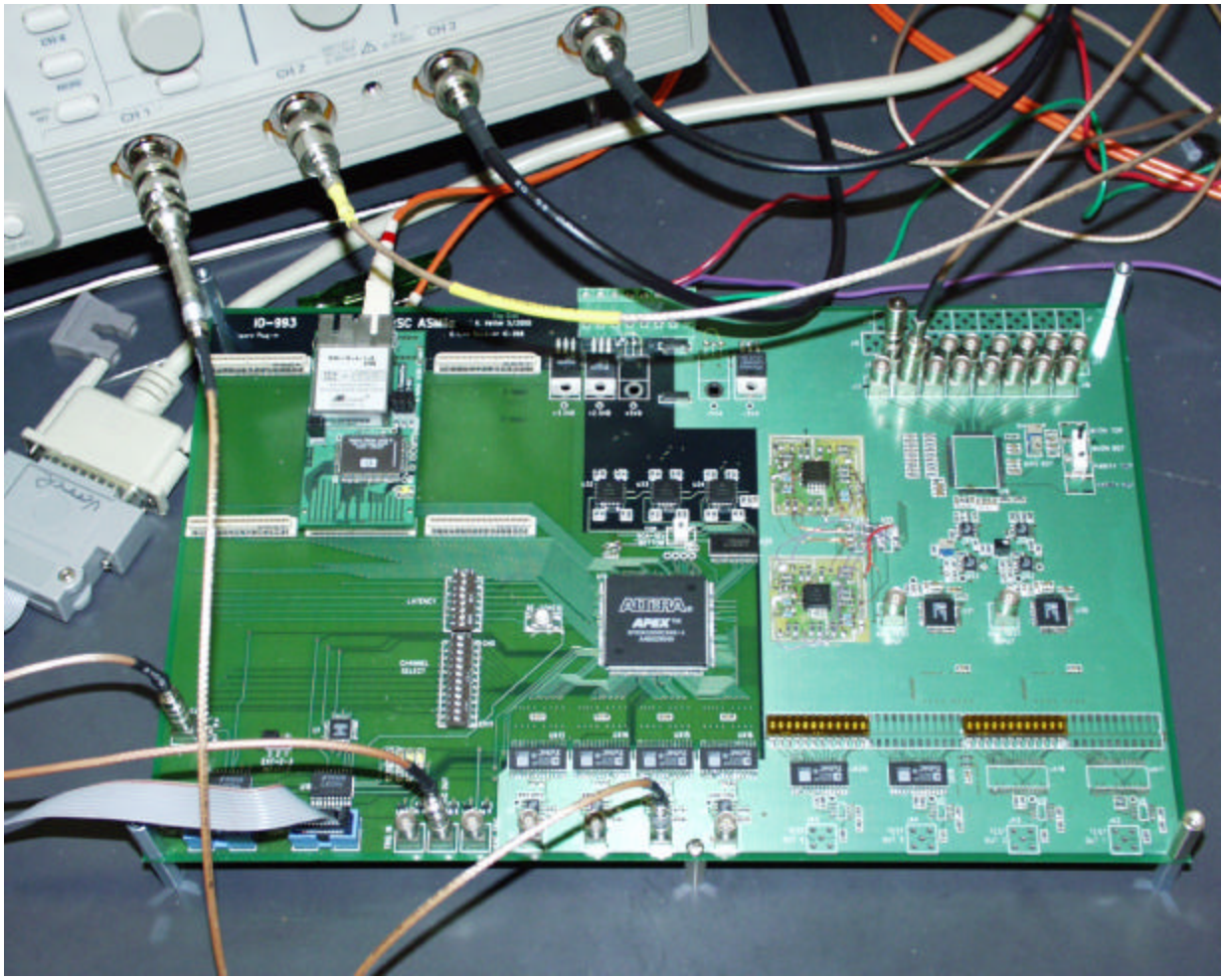
- Function: low-noise amplification and pulse shaping of the chamber signals
- No. of channels: 48
- No. of boards required: 640 (for 32 chambers)
- 60 x 210 mm board, 3.4W, plugs into chamber
- Design responsibility: BNL Instrumentation
- 12-channel prototypes tested with chamber, in beam, work fine
- 5 versions of this board plus flex connector in layout
- Milestones:
  - Module 0 fabrication 07/01
  - Module 0 beam test 09/01
  - Final Design Review 03/03
  - PRR 07/03
  - Production 08/03



ASM-2 board

- Function: analog memory, digitization, optical link
- No. of channels: 192
- No. of boards required: 160
- 120 x 430 mm board, 26W
- 50% more channels than LARG FEB in ¼ the area
- Design responsibility: BNL Instrumentation
- 12-channel prototype working on bench (ASM-2a)
  - Measure gain, linearity, noise, pedestal dispersion
  - Verify operation of G-link
  - Verify > 5MHz Read Clock rate
  - Verify interface to preamp/shaper
  - Implement trigger
- 96-channel version (ASM-2b) in design, for 9/01 beamtest
- Milestones:
  - ASM-2b fabrication 07/01
  - ASM-2b beam test 09/01
  - Final Design Review 03/03
  - PRR 07/03
  - Production 08/03

ASM-2 prototype



ROD

- Functions:
  - Generate control signals and transmit to chambers
  - Receive and process raw chamber data
  - Assemble events and transmit to Concentrator
  - Calibration and monitoring
  - ROD serves 2 chambers (1920 channels, 12.8 Gbit/s)
- Design responsibility: UCI
- No. of boards required: 16
- 9U VME plus 220 mm Transition Module, 100W
- Modular design using pluggable DSP-based GPU:
  - 70 x 70 mm, 3W
  - > 100 Mword/s data BW
  - Component cost ~ $300
  - 12 GPUs per ROD
- Status:
  - GPU: working prototype on hand
  - ROD: motherboard layout started 5/1/01
- Milestones:
  - Prelim. Design Review 05/01
  - First prototype in hand 08/01
  - Integration with ASM-2 04/02
  - Final design review 10/02
  - PRR 07/03

Concentrator

- Function: accept fully processed data from 16 (8) RODs, build ATLAS standard events, transmit to Trigger/DAQ
- Design responsibility: UCI
- No. required: 1 (2)
- Same board as ROD, different firmware and software
- Will be available same timeframe as ROD

Off-detector Support Electronics and Software

Support Electronics

- Function: interface CSC system to LHC and L1 timing, ATLAS Trigger/DAQ, physically support and supply power to RODs and Concentrators
- Design responsibility: UCI
- 1 9U VME crate per endcap
  - 16 RODs
  - 1 (2) Concentrator(s)
  - 1 TIM
  - 1 ROD Crate Controller
- Milestones:
  - Final DR 10/02
  - PRR 07/03

Software

- UCI responsibility
- Prelim. Design Review 08/03, Final 04/04

ASICs for CSC Electronics

CHIP	TYPE	FOUNDRY
• P/S	analog	Agilent
• SCA	mixed	DMILL
• MUX	digital	TBD
• POS. VREG	power	RHBip1

Preamp/Shaper (P/S)

- Technology: Agilent 0.5 um CMOS
- Location: ASM-1
- Function: 12-channel preamplifier and 7-pole shaper
- Design responsibility: BNL Instrumentation
- No. of chips required: 5,120 (full scope of 64 chambers)
- MPW runs: 3
- Tested with full size chambers in beam
- Radiation testing: preliminary ionizing test to 1 Mrad, very encouraging result
- Milestones:
  - Beam test 09/01
  - Final DR and PRR 10/01
  - Production 12/01

P/S Yield Issue

- Inconsistent yield on 3 MPW runs despite identical mask layout:
  - 1st run 2Q 1999: 45%
  - 2nd run 1Q 2000: 97%
  - 3rd run 1Q 2001: 84%
- All failures involve self-bias circuit (1 or 2 of 16 fail randomly) and are correctable by external forcing
- Suspected cause is pinholes in large on-chip decoupling capacitors
- Corrective actions:
  - External Design Rule Check by vendor
  - Simulate impact of removing on-chip caps
  - Revise design and submit for 2 more MPW runs
  - May delay PRR
- Minimum production run is expected to produce 14,000 die, so low yield is not a serious problem

SCA

- Technology: DMILL
- Location: ASM-2
- Function: analog memory
- Design responsibility: LARG
- No. chips required: 5,120 for full scope (64 chambers)
- This is the same chip used in LARG FEB
- Design was modified at our request to allow pin-selectable “MUON mode”
- Effectively increases the readout rate by X6
  - 4 channels x 3 gains => 12 channels
  - Duty cycle 50% => 100% per SCA
  - Read clock 5 MHz => 6.67 MHz
- Tested in MUON mode in lab, 3/01- 5/01
- LARG in control of radiation qualification, procurement, and production testing
- Production forseen for Jan. 02

MUX

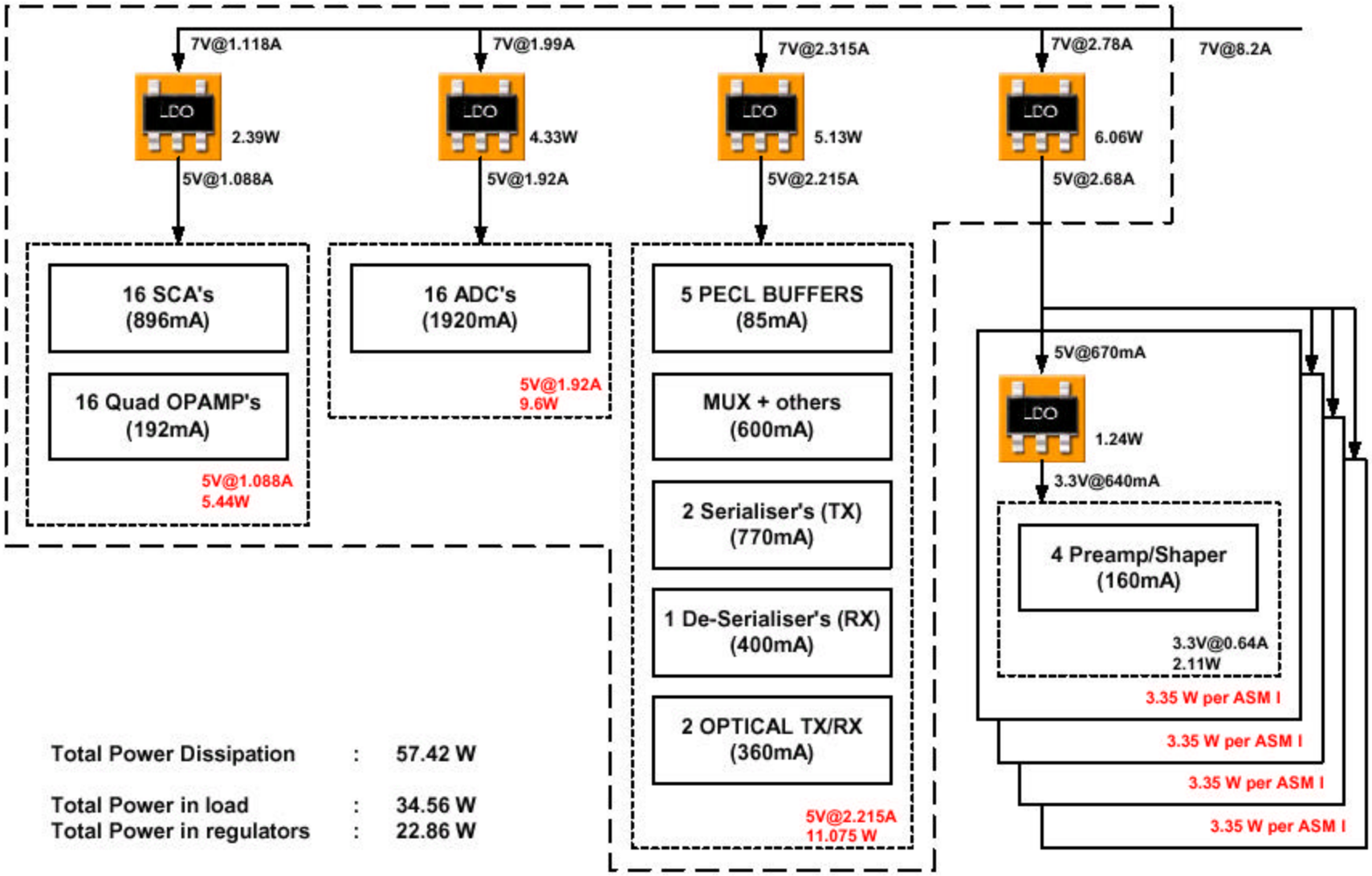
- Location: ASM-2
- Function: data concentration between ADC and G-link
- Technology: TBD
- No. of chips required: TBD
- Milestones:
  - Start design 10/01
  - MPW fab 02/02
  - Final DR 10/02?

Voltage regulator

- LHC4913 positive voltage regulator being developed in framework of RD-49 by ST Microelectronics Catania
- Location: ASM-1 and ASM-2
- Quantities required: 640 ea. 5V and 3.3V (for 32 chambers)

Low Voltage Power and Cabling

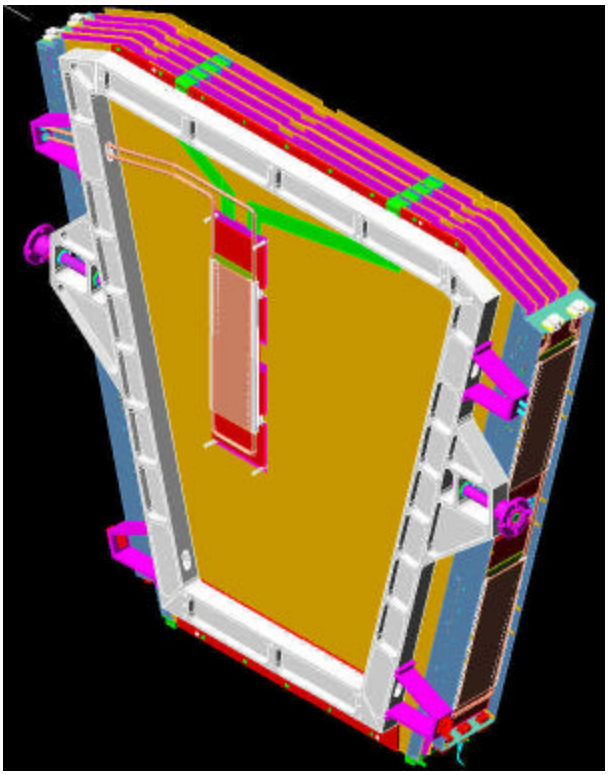
- Design for full scope (64 chambers)
- Uncertainties:
  - Power supply location
  - Cable run details
  - Local regulator characteristics
- Working assumptions:
  - Space for LV supplies available on UX15 floor
  - Use LARG-like supplies if neutron flux too high for standard DC-DC converters
  - 25m run to patch panel on outside of endcap wheel
  - 12 m from edge of endcap to chamber pigtail
- Total electronics power: 18400 W (2630A @ 7V)
- Cabling: 64 pairs AWG 4, 480 cm^2, 1000 kg
- 100 W dissipated per cable, 6400 W total for full scope
- Fiber optic cables
  - 960 fibers from USA15 (120m run)
  - 90 cm^2 cross section, 860 kg

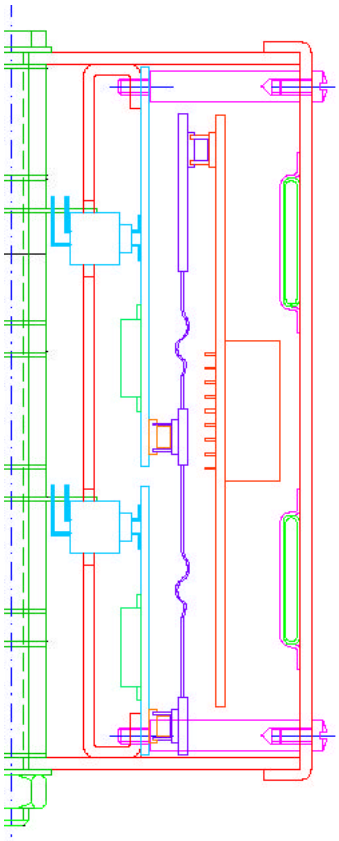


Total Power Dissipation	:	57.42 W
Total Power in load	:	34.56 W
Total Power in regulators	:	22.86 W

Faraday Cage

- Provides shielding, ground, cooling, and mechanical support for ASM-1 and ASM-2
- 2 FCs per chamber
- ASM-1 and ASM-2 boards require liquid cooling
  - Cooling plate with thermally conductive pads
- Design is in preliminary stage
- Space is constrained
- Need to finalize board layout, cable harness, and connector details
- Y-strip readout needs separate mechanics





Summary

- 2 of 3 ASICs are ready for production
- Schedule risk if MUX ASIC requires more than one iteration
- We rely on timely solution of ST voltage regulator problems
- Manpower concerns
  - ASM-2 design
  - FC
  - Test DAQ
  - Radiation qualification